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**Code No.: 21114 S**

# VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

**B.E. II Year (C.S.E.) I-Semester Supplementary Examinations, May/June-2017**

**Logic and Switching Theory**

Time: **3** hours Max. Marks: **70**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

***Part-A (10 X 2=20 Marks)***

1. Convert $(634)_8$ to binary.
2. Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction (i) X -Y and (ii) Y - X using 1's complements.
3. Implement the following Boolean function with NAND–NAND logic $F = \Sigma m(0,1,3,5)$.
4. Give the classification of logic families.
5. Design Half – adder using only NOR gates.
6. Write the design procedure for combinational circuits.
7. Write the excitation tables of JK and D flip flops.
8. What is race-around condition in a flip flop?
9. Draw the state diagram of MOD -10 counter.
10. Differentiate between ripple counters and synchronous counters.

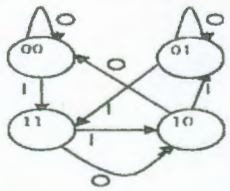
***Part-B (5 × 10 = 50 Marks)***

11. a) Construct an even parity seven bit code to transmit the data i)1010 ii)1110 [4]
    b) Show the truth table for each of the following functions and find its simplest POS form. [6]
    i) f(x,y,z) = xy+xz ii) f(x,y,z) = x'+yz'

12. a) Minimize the following expression using Tabulation procedure [5]
    $F(A,B,C,D) = \Sigma m(0,4,8,10,12,13,15) + d(1,2)$.
    b) Implement the following Boolean expression by OR-AND 2 level logic circuit. [5]
    F(x,y,z) = ((x+y').z)+(x'yz')

13. a) Design odd parity checker and generator circuits. [4]
    b) Implement the following function using suitable multiplexer F (A, B, C, D) = Σ(1, 3, 4, 11, 12, 13, 14 , 15) [6]

14. a) Draw the state diagram of a circuit that recognizes the sequence 1011. [4]
    b) Realize the circuit given in the following state diagram using JK Flip Flops. [6]




15. a) What is universal shift register? Explain its operation. [5]
    b) Design a 3-bit binary counter using T FF that has a repeated sequence of 6 states. 000-001-010-011-100-101-110. Give the state table, state diagram & logic diagram. [5]

16. a) Implement the given Boolean function using 8 : 1 multiplexer $F(x,y,z) = \Sigma(1, 3, 5, 6)$. [5]
    b) Reduce the following function using K-map technique $f(w, x, y, z) = \pi(0, 3, 4, 7, 8, 10, 12, 14) + d(2, 6)$. [5]

17. Answer any **two** of the following:
    a) Explain the working of carry look ahead adder circuit. [5]
    b) Differentiate Moore and Mealy machines with block diagram. [5]
    c) Draw the logic diagram of 3 bit binary up /down synchronous counter and explain with truth table. [5]

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